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EXAMINER LEE, CHUN KUAN				
ART UNIT 2181		PAPER NUMBER		
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

doctet1@thepatentattorneys.com
hholmes@thepatentattorneys.com
osteuball@thepatentattorneys.com

Office Action Summary

Application No.

10/777,368

Applicant(s)

RITZ ET AL.

Examiner

Chun-Kuan Lee

Art Unit

2181

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 February 2008.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5, 7-17 and 19-22 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-5, 7-17 and 19-22 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 12 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____

DETAILED ACTION

RESPONSE TO ARGUMENTS

1. Applicant's arguments with respect to claims 1-5, 7-17 and 19-22 have been considered but are moot in view of the new ground(s) of rejection. Currently, claims 6 and 18 are canceled, and claims 1-5, 7-17 and 19-22 are pending for examination.
2. In response to applicant's arguments (on page 8, last paragraph) regarding the rejection of amended independent claim 1 rejected under 35 U.S.C. 103(a) that the combination of references do not teach the access attribute in applicant's claimed invention because Kondratiev's table only indicates memory ranges that are allowed access and does not provide ability to directly specify a memory range that is not allow access; applicant's arguments have fully been considered, but are not found to be persuasive.

Please note that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

The examiner relied on Safranek for the teaching that a memory address page is not allow for access, and in combination with Kondratiev's table indicating memory ranges that are allowed access, the resulting combination of references further teaches the table indicating memory ranges that are allowed and not allowed access.

As similar arguments presented above for amended independent claim 1 are also applied towards amended independent claims 14, 17 and 21-22, the examiner will also apply the same response towards the amended independent claims 14, 17 and 21-22.

3. In response to applicant's arguments (on page 8, last paragraph) regarding the rejection of amended independent claim 1 rejected under 35 U.S.C. 103(a) that the combination of references do not teach the access attribute in applicant's claimed invention because Kondratiev's read and write access are indicated in two separate fields by specifying a memory address range in each of the two separate read memory range and write memory range; applicant's arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees, in view of applicant's arguments and in combination with the explanation from the interview conducted on 02/11/2008, that the singled filed is supported by the applicant's Figure 3 having a single column, Kondratiev does teach a single column (Fig. 2, ref. 210), wherein the single column includes read and write access in the sub-columns.

As similar arguments presented above for amended independent claim 1 are also applied towards amended independent claims 14, 17 and 21-22, the examiner will also apply the same response towards the amended independent claims 14, 17 and 21-22.

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4. In response to applicant's arguments (on page 10, 1st paragraph) regarding the rejection of amended independent claim 14 rejected under 35 U.S.C. 103(a) that the combination of Safranek and Kondratiev provide less control for memory access because the entire memory space is mapped for control of read and write access; applicant's arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees because the mapping of the entire memory space would provide more control for memory access, rather than lesser control.

I. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-5, 7-17 and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Safranek et al. (US Pub 2004/0193755) in view of Kondratiev et al. (US Patent 6,922,740).

6. As per claim 1, Safranek teaches a direct memory access memory corruption detection system embodied on a computer readable medium comprising the following computer executable components:

an access data store that stores access information (e.g. access information stored in NoDMA table 103 and NoDMA cache 109 of Fig 1) associated with memory (Fig. 1, ref. 101), the access data store comprising an access table (Fig. 1, ref. 103 and Fig. 3), the access table comprising an access attribute field, the access attribute field distinguishes no access to indicate no access ([0011]-[0021]; [0034] and [0038]); and

a memory controller (Fig. 1, ref. 117) that employs the access information to determine whether a requested direct memory access is permitted and rejects the requested direct memory access if it is not permitted (Fig. 4, ref. 417) and allows the requested direct memory access if it is permitted (Fig. 4, ref. 419) ([0014]-[0021]; [0034] and [0038]).

Safranek does not teach the computer readable medium comprising: a source identifier field and a memory address field; distinguishing between read, read and write, and write ... ; and a combination of source associated with the access attribute

Kondratiev teaches a system and a method comprising:

an access information comprising a source identifier field (e.g. device ID) and a memory address field (e.g. read access with memory address range, write access with memory address range) (Fig. 2, ref. 210 and col. 4, ll. 40-65); and

an access attribute distinguishing between read, read and write and write to indicate read, read and write or write for a combination of source associated with the access attribute and memory address range associated with the access attribute identified in the source identifier field (e.g. device ID) and memory address field (Fig. 2, ref. 210 and col. 4, ll. 40-65).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Kondratiev's device ID, and read and write access attribute with memory address range into Safranek's DMA memory corruption detection system for the benefit of increase security and reliability for accessing DMA (Kondratiev, col. 7, ll. 30-41) to obtain the invention as specified in claim 1.

7. As per claims 2-3, Safranek and Kondratiev teach all the limitation of claim 1 as discussed above, where Kondratiev further teaches the direct memory access memory corruption detection system comprising the access information comprising a direct memory access request, and wherein the direct memory access request comprising a transaction type (e.g. read-write access) (Kondratiev, Fig. 2 and col. 4, ll. 23-26).

8. As per claims 4-5, Safranek and Kondratiev teach all the limitation of claim 1 as discussed above, where Kondratiev further teaches the direct memory access memory corruption detection system comprising the direct memory access request comprising a source identifier (e.g. device ID), and wherein the source identifier being associated with a device (I/O device 140-1 of Fig. 1 and device ID of Fig. 2) (Kondratiev, col. 4, ll. 40-65).

9. As per claim 7, Safranek and Kondratiev teach all the limitation of claim 1 as discussed above, where Safranek further teaches the direct memory access memory corruption detection system comprising wherein the access information comprising at

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least one permitted memory address (Safranek, [0014] and [0021]), wherein certain segments of the memory do not have access restriction, therefore request for access are allowed.

10. As per claim 8, Safranek and Kondratiev teach all the limitation of claim 1 as discussed above, where Safranek further teaches the direct memory access memory corruption detection system comprising wherein the access information comprising at least one disallowed memory address (Safranek, [0014] and [0021]), wherein certain segments of the memory have access restriction, therefore request for access are denied.

11. As per claim 9, Safranek and Kondratiev teach all the limitation of claim 1 as discussed above, where Safranek further teaches the direct memory access memory corruption detection system comprising wherein the request comprising a read action or a write action (Safranek, [0015]).

12. As per claim 10, Safranek and Kondratiev teach all the limitation of claim 1 as discussed above, where Safranek further teaches the direct memory access memory corruption detection system comprising wherein the request comprising a peripheral component interface express bus transaction (Safranek, [0017] and [0019]).

13. As per claim 11, Safranek and Kondratiev teach all the limitation of claim 1 as discussed above, where Safranek further teaches the direct memory access memory corruption detection system comprising wherein the memory controller coupled to a device through a peripheral component interface express bus, the device providing the request (Safranek, [0017] and [0019]).

14. As per claim 12, Safranek and Kondratiev teach all the limitation of claim 1 as discussed above, where Safranek further teaches the direct memory access memory corruption detection system comprising wherein the memory controller further providing error information, if the requested direct memory access is not permitted (Safranek, Fig. 4; [0034] and [0038]), wherein the error is logged and can be utilized for subsequent analyzing.

15. As per claim 13, Safranek and Kondratiev teach all the limitation of claim 12 as discussed above, where Safranek further teaches the direct memory access memory corruption detection system comprising the error information comprising source information associated with the requested direct memory access (Safranek, Fig. 4; [0034] and [0038]).

16. As per claim 14, Safranek teaches a direct memory access memory corruption detection system embodied on a computer readable medium comprising the following computer executable components:

a memory controller (Fig. 1, ref. 117) that includes an access data store comprising an access table (Fig. 1, ref. 103, 109 and Fig. 3), the access table comprising an access attribute field, the access attribute field contains an access attribute that distinguishes no access to indicate no access, wherein the access attribute contains data indicating no access when the access attribute is not permitted access to a memory page associated with the access attribute (Fig. 4; [0011]-[0021]; [0034] and [0038]); and

the memory controller (Fig. 1, ref. 117) employs the access information to determine whether a requested direct memory access is permitted and rejects the requested direct memory access if it is not permitted (Fig. 4, ref. 417) and allows the requested direct memory access if it is permitted (Fig. 4, ref. 419) ([0014]-[0021]; [0034] and [0038]).

Safranek does not teach the computer readable medium comprising: a source identifier field and a memory address field; distinguishing between read, read and write, and write, to indicate read, read and write, and write ... , wherein the access attribute contains data indicating read ..., wherein the access attribute contains data indicating write ..., wherein the access attribute contains data indicating read and write ... ; and a device driver

Kondratiev teaches a system and a method comprising:

an access information comprising a source identifier field (e.g. device ID) and a memory address field (e.g. read access with memory address range, write access with memory address range) (Fig. 2, ref. 210 and col. 4, ll. 40-65);

an access attribute distinguishing between read, read and write and write to indicate read, read and write or write for a combination of source associated with the access attribute and memory address range associated with the access attribute identified in the source identifier field (e.g. device ID) and memory address field (Fig. 2, ref. 210 and col. 4, ll. 40-65);

wherein the access attribute contains data indicating read when the source identified by the source identifier associated with the access attribute is only permitted to read the memory address range associated with the access attribute (Fig. 2, ref. 210 and col. 4, ll. 40-65), as the access attribute provide only read access range,

wherein the access attribute contains data indicating write when the source identified by the source identifier associated with the access attribute is only permitted to write to the memory address range associated with the access attribute (Fig. 2, ref. 210 and col. 4, ll. 40-65), as the access attribute provide only write access range,

wherein the access attribute contains data indicating read and write when the source identified by the source identifier associated with the access attribute is permitted to read and write to the memory address range associated with the access attribute (Fig. 2, ref. 210 and col. 4, ll. 40-65), as the access attribute provide read and write access range; and

a device driver (e.g. bus master) that programs (e.g. program by invoking a function to request DMA access) a device for a direct memory access operation, and provides the access information to the memory controller via a direct memory access application interface (col. 4, ll. 6-26 and col. 6, ll. 43-53).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Kondratiev's device ID, read and write access attribute with memory address range and the bus master into Safranek's DMA memory corruption detection system, wherein the combination of Safranek and Kondratiev further teaches:

wherein the source identified by the source identifier associated with the access attribute is not permitted access to the memory address range associated with the access attribute (Safranek, Fig. 4; [0011]-[0021]; [0034]; [0038] and Kondratiev, Fig. 2, ref. 210 and col. 4, ll. 40-65),

for the benefit of increase security and reliability for accessing DMA (Kondratiev, col. 7, ll. 30-41) to obtain the invention as specified in claim 14.

17. As per claim 15, Safranek and Kondratiev teach all the limitations of claim 14 as discussed above, where Kondratiev further teaches the direct memory access memory corruption detection system further comprising the stored access information comprising a range of physical memory (access range), a source identifier (device ID), and an access attribute (read and write) (Kondratiev, Fig. 2).

18. As per claim 16, Safranek and Kondratiev teach all the limitations of claim 14 as discussed above, where Safranek teaches the direct memory access memory corruption detection system comprising wherein the request comprising a peripheral component interface express bus transaction (Safranek, [0017] and [0019]).

19. As per claim 17, Safranek teaches a method that facilitates detection of direct memory access memory corruption comprising:

receiving a request for a direct memory access transaction, the request comprising a least one memory address ([0014]-[0021] and [0034]);

determining whether the request is permitted based, at least in part on, stored access information (Fig. 1, ref. 103, 109 and Fig. 3) and the request, the stored access information comprising at least one access attribute, an access attribute distinguishes no access to indicate no access (Fig. 4; [0011]-[0021]; [0034] and [0038]); and

rejecting the requested direct memory access if it is not permitted (Fig. 4, ref. 417) and allowing the direct memory access if it is permitted (Fig. 4, ref. 419) ([0014]-[0021]; [0034] and [0038]).

Safranek does not teach the method comprising: the request comprising a source identifier, and an access attribute; at least one source identifier and at least one memory address range; and distinguishes between read, read and write, and write to indicate read, read and write, or write

Kondratiev teaches a system and a method comprising:

a request including a source identifier (e.g. device ID), and an access attribute (e.g. read, write) (Fig. 2 and col. 3, l. 51 to col. 4, l. 65);

an access information comprising at least one source identifier (e.g. device ID) and at least one memory address range (e.g. read access with memory address range, write access with memory address range) (Fig. 2, ref. 210 and col. 4, ll. 40-65); and

an access attribute distinguishing between read, read and write and write to indicate read, read and write or write for a combination of source associated with the access attribute and memory range associated with the access attribute identified by the at least one source identifier and at least one memory address range (Fig. 2, ref. 210 and col. 4, ll. 40-65).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Kondratiev's device ID, read and write access attribute with memory address range and the bus master into Safranek's DMA memory corruption detection system for the benefit of increase security and reliability for accessing DMA (Kondratiev, col. 7, ll. 30-41) to obtain the invention as specified in claim 17.

20. As per claim 19, Safranek and Kondratiev teach all the limitations of claim 17 as discussed above, where Kondratiev further teaches the method that facilitates detection of direct memory access memory corruption comprising storing access information in an access data store, the access information comprising a source identifier (device ID), at least one memory address (access range) and an access attribute (read and write) (Kondratiev, ACL 210 Fig. 2).

21. As per claim 20, Safranek and Kondratiev teach all the limitations of claim 17 as discussed above, where Safranek further teaches the method that facilitates detection of direct memory access memory corruption comprising a computer readable medium

having stored thereon computer executable instructions for carrying out the method (Safranek, [0039]).

22. As per claim 21, Safranek teaches a data packet transmitted between two or more components embodied on a computer readable medium that facilitates detection of direct memory access memory corruption, the data packet comprising:

a data field comprising a corrected platform error event ([0034] and [0038]), the corrected platform error event being based, at least in part, upon a determination that a requested direct memory access is not permitted ([0034] and [0038]), the determination being based, at least in part, upon access information stored in an access table (Fig. 1, ref. 103, 109 and Fig. 3) and the requested direct memory access (Fig. 4; [0011]-[0021]; [0034] and [0038]), the access information comprising at least one access attribute, the at least one access attribute distinguishes no access to indicate no access (Fig. 4; [0011]-[0021]; [0034] and [0038]).

Safranek does not teach the system comprising: at least one source identifier and at least one memory address range; and distinguishing from amongst read, read and write, and write to indicate read, read and write, or write

Kondratiev teaches a system and a method comprising:

an access information comprising at least one source identifier (e.g. device ID) and at least one memory address range (e.g. read access with memory address range, write access with memory address range) (Fig. 2, ref. 210 and col. 4, ll. 40-65); and

an access attribute distinguishes from amongst read, read and write, and write to indicate read, read and write, or write for a combination of source and memory address range identified by the at least one source identifier and at least one memory address range associated with the at least one access attribute (Fig. 2, ref. 210 and col. 4, ll. 40-65).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Kondratiev's device ID, and read and write access attribute with memory address range into Safranek's DMA memory corruption detection system for the benefit of increase security and reliability for accessing DMA (Kondratiev, col. 7, ll. 30-41) to obtain the invention as specified in claim 21.

23. As per claim 22, Safranek teaches a direct memory access memory corruption detection system embodied on a computer readable medium comprising:

means for storing access information (Fig. 1, ref. 103, 109 and Fig. 3) associated with memory (Fig. 1, ref. 101) ([0011]-[0021]);

means for receiving a request for a direct memory access ([0014]-[0021] and [0034]);

means for determining whether a requested direct memory access is permitted based, at least in part, upon the stored access information and the request, the stored access information comprising at least one access attribute, the at least one access attribute distinguishes no access to indicate no access (Fig. 4; [0011]-[0021]; [0034] and [0038]); and,

means for rejecting the requested direct memory access if it is not permitted (Fig. 4, ref. 417) and allowing the direct memory access if it is permitted (Fig. 4, ref. 419) ([0014]-[0021]; [0034] and [0038]).

Safranek does not teach the system comprising: at least one source identifier and at least one memory address range; and distinguishes between read, read and write, and write to indicate one of read, read and write, or write

Kondratiev teaches a system and a method comprising:

an access information comprising at least one source identifier (e.g. device ID) and at least one memory address range (e.g. read access with memory address range, write access with memory address range) (Fig. 2, ref. 210 and col. 4, ll. 40-65); and

an access attribute distinguishes between read, read and write, and write to indicate one of read, read and write, or write for a combination of source and memory address range identified by the at least one source identifier and at least one memory address range associated with the at least one access attribute (Fig. 2, ref. 210 and col. 4, ll. 40-65).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Kondratiev's device ID, and read and write access attribute with memory address range into Safranek's DMA memory corruption detection system for the benefit of increase security and reliability for accessing DMA (Kondratiev, col. 7, ll. 30-41) to obtain the invention as specified in claim 22.

II. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

IMPORTANT NOTE

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

March 24, 2008

Chun-Kuan (Mike) Lee
Examiner
Art Unit 2181

/Alford W. Kindred/

Supervisory Patent Examiner, Art Unit 2163